IN THE SPECIFICATION:

Please amend paragraph [0009] as follows:

The present invention is concerned with an electronic parts packaging structure, which comprises a wiring substrate including a predetermined wiring pattern; an electronic parts [[a]] connection terminal on an element forming surface of which is flip-chip connected to the wiring pattern; an insulating film for covering the electronic parts; a via hole formed in a predetermined portion of the electronic parts and the insulating film on the connection terminal; and an overlying wiring pattern formed on the insulating film and connected to the connection terminal via the via hole.

Please amend paragraph [0012] as follows:

In one preferred [[mode]] embodiment of the present invention, [[the]] a semiconductor chip whose thickness is ~~thinned~~ reduced to about 150 μm or less is used as the electronic parts. Also, the same structural body as the electronic parts, the insulating film, and the overlying wiring pattern, which are formed on the wiring pattern of the wiring substrate, may be repeated n times (n is an integer of 1 or more) on the overlying wiring pattern in a multi-layered fashion, and a plurality of electronic parts may be connected mutually via the via holes.

Please amend paragraph [0013] as follows:

In this case, [[since]] because a total thickness of the electronic parts packaging structure

can be reduced, such a packaging structure can ~~respond to~~ be formed with a higher density. In addition, [[since]] because upper and lower electronic parts are connected mutually via the wirings in the vertical direction, a length of the wiring can be shortened rather than the case that the semiconductor chips are connected via wires or the case that the wirings accompanied by the wiring routing in the lateral direction are provided. As a result, the semiconductor device in the high-frequency application can respond to a higher speed of the signal speed.

Please amend paragraph [0014] as follows:

Also, the present invention is concerned with a method of manufacturing an electronic parts packaging structure, which comprises the steps of flip-chip connecting a connection terminal of [[an]] electronic parts having the connection terminal on an element forming surface to a wiring pattern formed on or over a base substrate; forming an insulating film for covering the electronic parts; forming a via hole having a depth that reaches the connection terminal by etching a predetermined portion from an upper surface of the insulating film to the element forming surface of the electronic parts; and forming an overlying wiring pattern, which is connected to the connection terminal via the via hole, on the insulating film.

Please amend paragraph [0016] as follows:

In one preferred [[mode]] embodiment of the present invention, the step of forming the overlying wiring pattern includes the steps of forming a resist film having an opening portion in a

predetermined portion containing the via hole on the insulating film, forming a conductive film pattern in the via hole and the opening portion of the resist film by applying a plating upward from the connection terminal exposed from a bottom portion of the via hole by means of electroplating that utilizes the wiring pattern and the connection terminal of the electronic parts connected to the wiring pattern as a plating power-supply layer, and removing the resist film to get the overlying wiring pattern.

Please amend paragraph [0017] as follows:

By doing [[in]] this [[way]], in the step of forming the conductive film patterns in the via holes and the opening portions of the resist film, the conductive film patterns are formed by applying sequentially a plating upward from the connection terminals that are exposed from the bottom portions of the via holes. Therefore, the conductive film patterns are filled and formed without generation of the voids in the via holes. As a result, [[since]] because the reliability of the connection between the connection terminals of the electronic parts and the overlying wiring patterns via the via holes can be improved, yield of the production of the electronic parts packaging structure can be improved.

Please amend paragraph [0025] as follows:

Then, as shown in FIG. 1D, the resist film 12 is removed. Then, an inorganic insulating film 14 made of a silicon oxide film, or the like is formed on inner surfaces of the via holes 10b

and the back surface of the semiconductor wafer 10 by the CVD, or the like. Then, the inorganic insulating film 14 is removed from bottom portions of the via holes 10b by [[the]] laser, or the like. Thus, the connection pad 10a (the portion indicated by A in FIG. 1D) is exposed from the bottom portions of the via holes 10b. The inorganic insulating film 14 is formed to isolate conductors filled in the via holes 10b from the semiconductor wafer 10.

Please amend paragraph [0026] as follows:

Then, as shown in FIG. 1E, a seed Cu film (not shown) is formed on the inner surfaces of the via holes 10b and the back surface of the semiconductor wafer 10 by the electroless plating or the sputter method. Then, the resist film 12 having the opening portions 12a at predetermined portions containing the via holes 10b is formed on the seed Cu film. Then, Cu film patterns 16a are formed in the via holes 10b and the opening portions 12a of the resist film 12 by [[the]] electroplating utilizing the seed Cu film as the plating power-supply layer.

Please amend paragraph [0036] as follows:

In the electronic parts packaging structure 1 of the first embodiment, the semiconductor chip 20 a thickness of which is ~~thinned~~ reduced to about 150 μm (preferably about 50 μm) is flip-chip connected to the second wiring patterns 32a while such chip is buried in the second interlayer insulating film 34a. Then, the via holes 10b are formed in the semiconductor chip 20, and then the connection pads 10a on the element forming surface are connected to the through

electrodes 16 on the back surface via the via holes 10b. Also, the via holes 34y are formed in the second interlayer insulating film 34a that covers the semiconductor chip 20, and then the third wiring patterns 32b connected to the through electrodes 16 via the via holes 34y are formed.

Please amend paragraph [0037] as follows:

In addition, a plurality of semiconductor chips 20 each having [[the]] a similar structure may be stacked three-dimensionally as a multi-layered structure, and then these semiconductor chips 20 may be connected mutually via the through electrodes 16 formed in these chips and the via holes formed in the interlayer insulating films.

Please amend paragraph [0043] as follows:

The manufacturing equipments employed in the above RIE step (or the laser step) and the electroplating step are relatively expensive. Therefore, if the ~~man-hour~~ man-hours of the RIE or the electroplating [[is]] are increased [[like]] as in the first embodiment, heavy equipment investments are by necessity required, and as a result the situation ~~to result~~ results in an increase in production cost ~~may be supposed~~. In addition, in some case such a disadvantage is caused that, [[since]] because the manufacturing ~~man-hour is~~ man-hours are increased, the appointed date of delivery is delayed.